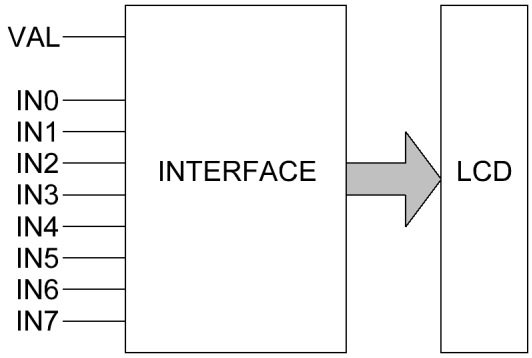
T.D. 6
Interface LCD

On désire réaliser une petite interface LCD permettant d'afficher un certain nombre de messages prédéfinis. Cette interface sera constituée des éléments suivants :

- un afficheur LCD alphanumérique à contrôleur intégré ;
- une EPROM **M27128A** ;
- un compteur **74HCT4060** ;
- un verrou **74HCT373**.

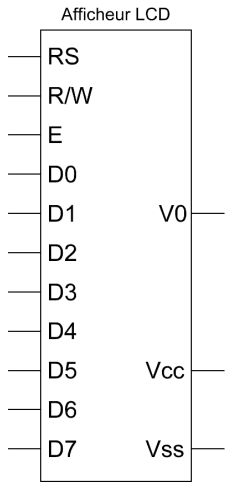
Les différents messages seront stockés dans l'EPROM. La sélection du message à afficher se fera à l'aide de 8 lignes d'entrée, de $\mathbf{IN_0}$ à $\mathbf{IN_7}$, laissant un choix de 256 messages. Une entrée **VAL** servira à la validation du message à afficher.



VAL = 0 → Les entrées $\mathbf{IN_0}$ à $\mathbf{IN_7}$ ne sont pas prises en compte. Pas de changement sur l'écran LCD.

VAL = 1 → Le message affiché est celui sélectionné par les entrées $\mathbf{IN_0}$ à $\mathbf{IN_7}$.

Fonctionnement de l'afficheur LCD



RS	0 = Caractère de commande. 1 = Caractère ASCII.
R/W	0 = Écriture d'un caractère. 1 = Lecture d'un caractère.
E	Validation du bus de donnée. (La validation s'effectue sur front descendant.)
$\mathbf{D_{7:0}}$	Bus de donnée bidirectionnel.
$\mathbf{V_0}$	Tension de réglage du contraste ($V_{SS} \leq V_0 \leq V_{CC}$).
$\mathbf{V_{CC}}$ $\mathbf{V_{SS}}$	Alimentation de l'afficheur.

Tension de seuil des entrées à $V_{CC}/2$.

L'afficheur LCD possède un contrôleur intégré qui facilite la gestion de l'affichage. Ce contrôleur permet non seulement d'afficher des caractères, mais aussi d'exécuter des commandes. Les informations présentes sur son bus de donnée peuvent donc être de deux types : le code ASCII d'un caractère à afficher ou une commande à exécuter. Les commandes disponibles sont détaillées dans le tableau ci-dessous :

Commandes de l'afficheur LCD	
38	Affichage sur 2 lignes en mode 8 bits.
0C	Le curseur est masqué.
06	Affichage du texte de gauche à droite.
80	Place le curseur au début de la ligne 1.
C0	Place le curseur au début de la ligne 2.
FF	Aucun effet.

Format des messages et contenu de l'EPROM

L'EPROM contient 256 messages numérotés de 0 à 255. Chaque message est composé de 64 octets que l'on peut décomposer en quatre blocs :

- Bloc 0 : 16 octets de commande.
- Bloc 1 : 16 octets au format ASCII qui seront affichés sur la ligne 1 de l'afficheur.
- Bloc 2 : 16 octets de commande.
- Bloc 3 : 16 octets au format ASCII qui seront affichés sur la ligne 2 de l'afficheur.

Le tableau ci-dessous donne un aperçu du contenu de la mémoire :

Message	**Bloc**	**Adresse**	**Contenu de la mémoire**
0	0	0000	FF FF FF FF FF FF FF FF FF FF FF FF 38 0C 06 80
	1	0010	**Codes ASCII ligne 1**
	2	0020	FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF C0
	3	0030	**Codes ASCII ligne 2**
1	0	0040	FF FF FF FF FF FF FF FF FF FF FF FF 38 0C 06 80
	1	0050	**Codes ASCII ligne 1**
	2	0060	FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF C0
	3	0070	**Codes ASCII ligne 2**
...	...	...	...
255	0	3FC0	FF FF FF FF FF FF FF FF FF FF FF FF 38 0C 06 80
	1	3FD0	**Codes ASCII ligne 1**
	2	3FE0	FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF C0
	3	3FF0	**Codes ASCII ligne 2**

1. Décomposez le bus d'adresse de l'EPROM en trois champs de bits. Chacun des champs contiendra respectivement :
   - la position d'un octet à l'intérieur d'un bloc ;
   - le numéro d'un bloc à l'intérieur d'un message ;
   - le numéro d'un message.

2. La capture d'écran ci-dessous est obtenue lors de l'affichage du message 130 :

```
Erreur :
Division par 0.
```

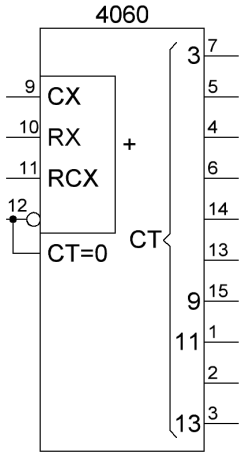
   Remplissez le tableau suivant qui donne le contenu de la mémoire pour le message 130 :

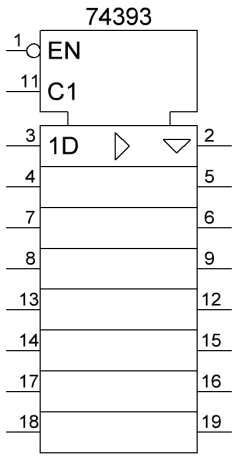
Adresse	**Contenu de la mémoire**															

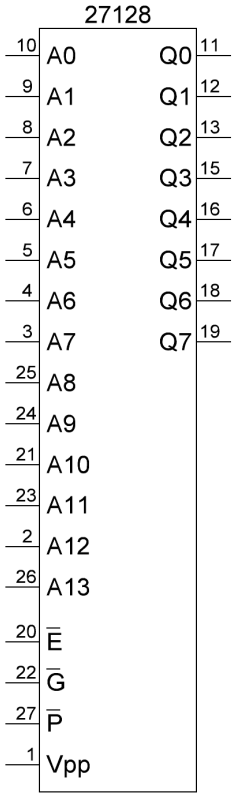
3. À l'aide de la documentation technique de la mémoire, câblez son bus de commande.
4. Câblez le bus de donnée de la mémoire.
5. Câblez l'entrée **R/W** de l'afficheur LCD.
6. À l'aide de la documentation technique du compteur, donnez une brève description de son fonctionnement.
7. À chaque front descendant de la sortie 3 du compteur (broche 7), un caractère du message en cours d'affichage doit être transmis à l'afficheur. Câblez l'entrée **E** de l'afficheur LCD ainsi que les entrées $\mathbf{A_0}$ à $\mathbf{A_5}$ de la mémoire.
8. Câblez l'entrée **RS** de l'afficheur LCD.
9. Terminez le câblage de l'afficheur LCD de façon à pouvoir ajuster la tension $\mathbf{V_0}$.
10. Afin de donner l'illusion que tous les caractères d'un message s'affichent simultanément, les 64 octets constituant un message doivent être envoyés à l'afficheur en moins de 40 ms. Donnez la fréquence minimale à appliquer au compteur.
11. Câblez les entrées du compteur afin d'obtenir une fréquence d'oscillation voisine de celle obtenue dans la question précédente.
12. Après qu'une adresse valide a été positionnée sur son bus d'adresse, la mémoire a besoin d'un certain temps avant de fournir une donnée valide sur son bus de donnée. Trouvez, à l'aide de sa documentation technique, le temps maximal dont la mémoire a besoin. Quel problème cela peut-il poser ?
13. Afin de résoudre ce problème, on propose de retarder le signal arrivant sur l'entrée **E** d'environ 10 µs. Donnez le nouveau schéma de câblage sachant que le temps de charge d'un condensateur à travers une résistance est :

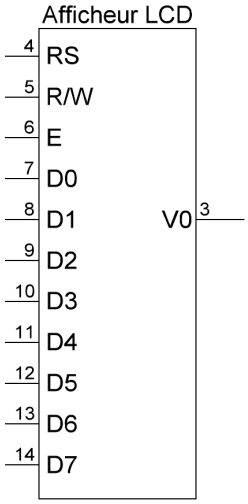
$$T_{charge} = R.C.ln(\frac{V_{CC} - V_{départ}}{V_{CC} - V_{arrivée}})$$

14. Câblez le verrou afin de réaliser la validation du message à l'aide d'une entrée **VAL** puis précisez l'emplacement des entrées $\mathbf{IN_0}$ à $\mathbf{IN_7}$.


4060
9 CX
10 RX
11 RCX
12
CT=0
+
CT
3 7
5
4
6
14
13
9 15
11 1
2
13 3


74393
1 EN
11 C1
3 1D
2
4
5
7
6
8
9
13
12
14
15
17
16
18
19


27128
10 A0
9 A1
8 A2
7 A3
6 A4
5 A5
4 A6
3 A7
25 A8
24 A9
21 A10
23 A11
2 A12
26 A13
20 Ē
22 Ḡ
27 P̄
1 Vpp
Q0 11
Q1 12
Q2 13
Q3 15
Q4 16
Q5 17
Q6 18
Q7 19

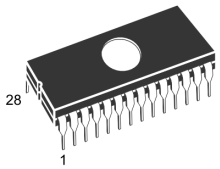

Afficheur LCD
4 RS
5 R/W
6 E
7 D0
8 D1
9 D2
10 D3
11 D4
12 D5
13 D6
14 D7
V0 3

SGS-THOMSON MICROELECTRONICS

M27128A

NMOS 128K (16K x 8) UV EPROM

- FAST ACCESS TIME: 200ns
- EXTENDED TEMPERATURE RANGE
- SINGLE 5 V SUPPLY VOLTAGE
- LOW STANDBY CURRENT: 40mA max
- TTL COMPATIBLE DURING READ and PROGRAM
- FAST PROGRAMMING ALGORITHM
- ELECTRONIC SIGNATURE
- PROGRAMMING VOLTAGE: 12V



FDIP28W (F)

DESCRIPTION

The M27128A is a 131,072 bit UV erasable and electrically programmable memory EPROM. It is organized as 16,384 words by 8 bits.

The M27128A is housed in a 28 Pin Window Ceramic Frit-Seal Dual-in-Line package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

Figure 1. Logic Diagram

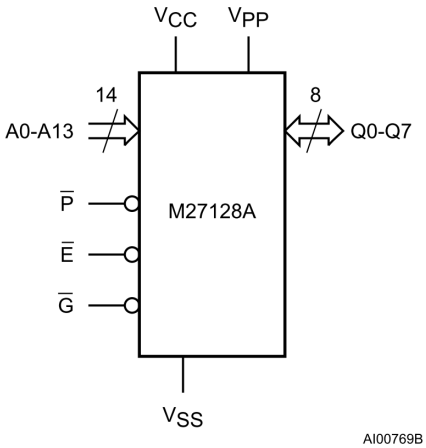


Table 1. Signal Names

A0 - A13	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

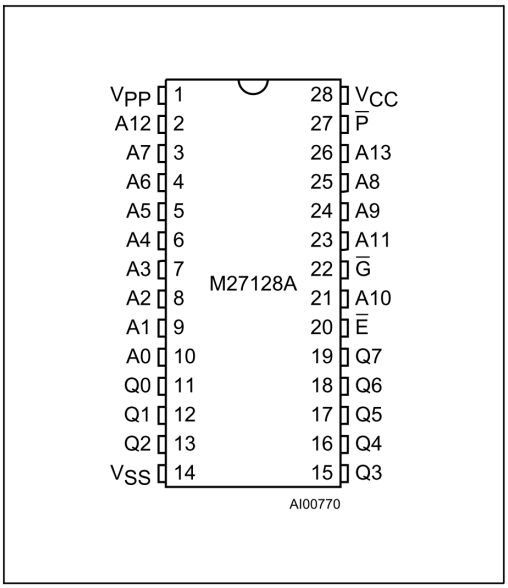
March 1995

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias	grade 1 grade 6	–10 to 80 –50 to 95	°C
T_{STG}	Storage Temperature		–65 to 125	°C
V_{IO}	Input or Output Voltages		–0.6 to 6.25	V
V_{CC}	Supply Voltage		–0.6 to 6.25	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Figure 2. DIP Pin Connections



DEVICE OPERATION

The seven modes of operation of the M27128A are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27128A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection.

Assuming that the addresses are stable, address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the outputs after the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27128A has a standby mode which reduces the maximum active power current from 85mA to 40mA. The M27128A is placed in the standby mode by applying a TTL high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

DEVICE OPERATION (cont'd)

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus.

This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of fast EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of this transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPPROM), all bits of the M27128A are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The M27128A is in the programming mode when V_{PP} input is at 12.5V and $\overline{E}$ and $\overline{P}$ are at TTL low. The data to be programmed is applied 8 bits in parallel, to the data output pins. The levels required for the address and data inputs are TTL.

Fast Programming Algorithm

Fast Programming Algorithm rapidly programs M27128A EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each byte is

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	V_{IH}	X	V_{CC}	Data Out
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	V_{CC}	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL} Pulse	X	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	X	X	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes Out

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5%.

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	1	0	0	0	1	0	0	1	89h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

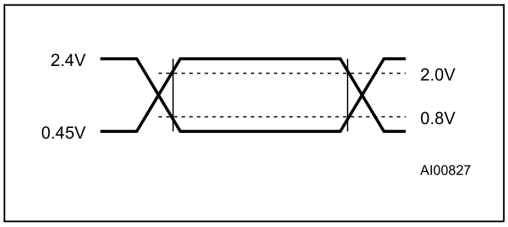


Figure 4. AC Testing Load Circuit

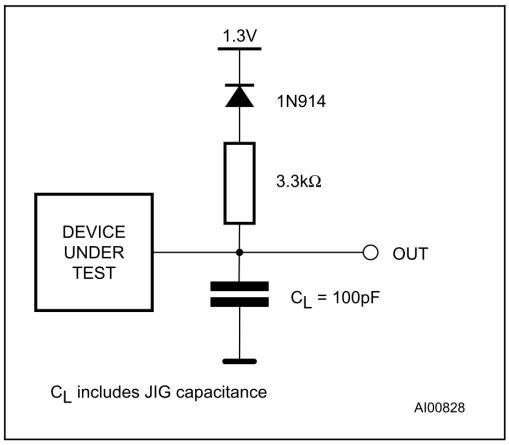


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	=	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	=	12	pF

Note: 1. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

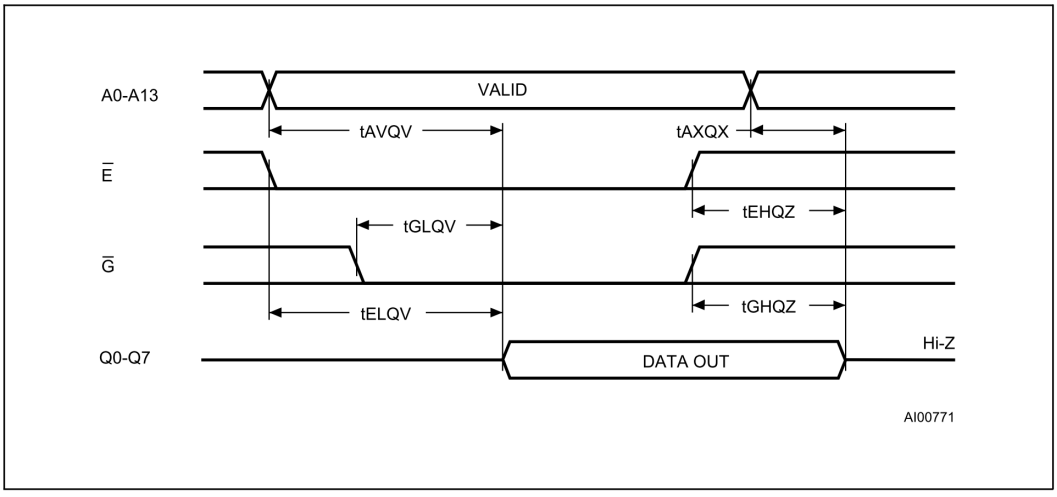


Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		75	mA
I_{CC1}	Supply Current (Standby)	$\overline{E} = V_{IH}$		35	mA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		5	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA	=	0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 7. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27128A								Unit
				-2, -20		blank, -25		-3, -30		-4		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		200		250		300		450	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		200		250		300		450	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		75		100		120		150	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	55	0	60	0	105	0	130	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	55	0	60	0	105	0	130	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

74HC373; 74HCT373

Octal D-type transparent latch; 3-state

Rev. 4 — 3 September 2010 Product data sheet

1. General description

The 74HC373; 74HCT373 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL. It is specified in compliance with JEDEC standard no. 7A.

The 74HC373; 74HCT373 is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all latches.

The 74HC373; 74HCT373 consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the Dn inputs enters the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D input changes.

When LE is LOW the latches store the information that was present at the D inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the 8 latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The 74HC373; 74HCT373 is functionally identical to:

- 74HC563; 74HCT563: but inverted outputs and different pin arrangement
- 74HC573; 74HCT573: but different pin arrangement

2. Features and benefits

- 3-state non-inverting outputs for bus oriented applications
- Common 3-state output enable input
- Functionally identical to the 74HC563; 74HCT563 and 74HC573; 74HCT573
- ESD protection:
  - HBM JESD22-A114F exceeds 2 000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from −40 °C to +85 °C and from −40 °C to +125 °C

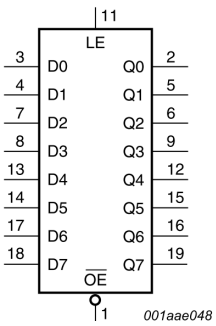


Fig 2. Logic symbol

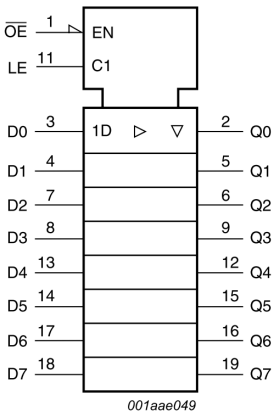


Fig 3. IEC logic symbol

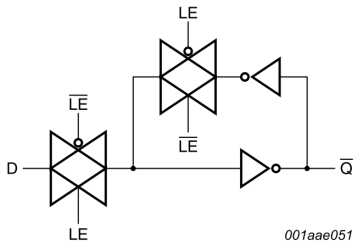


Fig 4. Logic diagram (one latch)

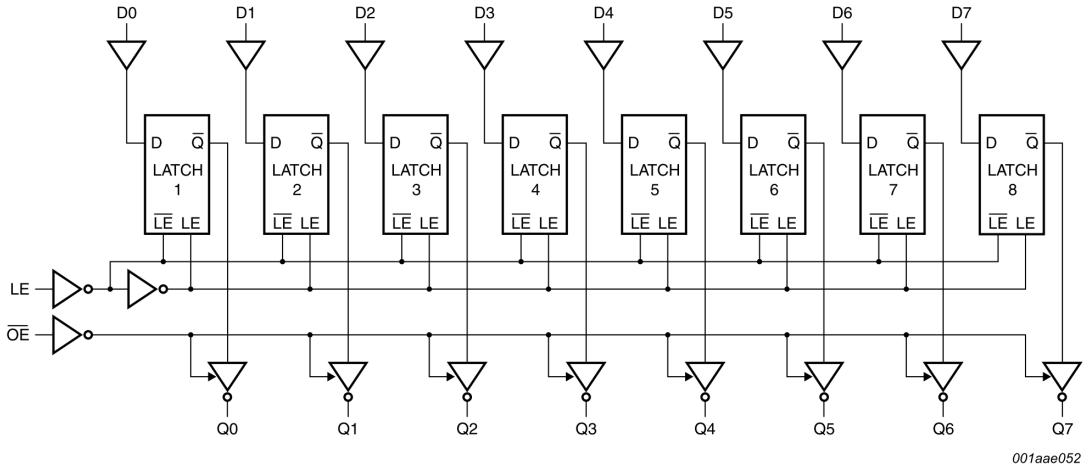


Fig 5. Logic diagram

5. Pinning information

5.1 Pinning

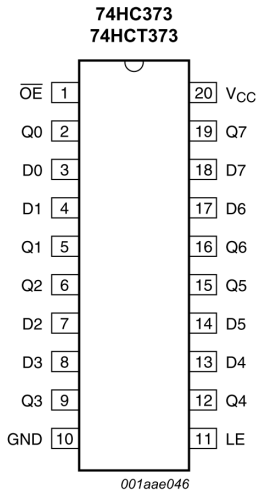
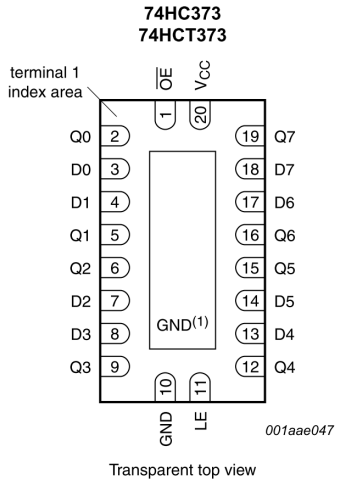


Fig 6. Pin configuration DIP20, SO20, SSOP20 and TSSOP20



Transparent top view

(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as supply pin or input.

Fig 7. Pin configuration DHVQFN20

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{OE}$	1	3-state output enable input (active LOW)
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	2, 5, 6, 9, 12, 15, 16, 19	3-state latch output
D0, D1, D2, D3, D4, D5, D6, D7	3, 4, 7, 8, 13, 14, 17, 18	data input
GND	10	ground (0 V)
LE	11	latch enable input (active HIGH)
V_{CC}	20	supply voltage

74HC4060; 74HCT4060

14-stage binary ripple counter with oscillator

Rev. 03 — 14 July 2008 Product data sheet

1. General description

The 74HC4060; 74HCT4060 are high-speed Si-gate CMOS device and is pin compatible with the HEF4060.

The 74HC4060; 74HCT4060 are 14-stage ripple-carry counter/dividers and oscillators with three oscillator terminals (RS, RTC and CTC), ten buffered outputs (Q3 to Q9 and Q11 to Q13) and an overriding asynchronous master reset (MR). The oscillator configuration allows design of either RC or crystal oscillator circuits. The oscillator may be replaced by an external clock signal at input RS. In this case keep the other oscillator pins (RTC and CTC) floating. The counter advances on the negative-going transition of RS. A HIGH level on MR resets the counter (Q3 to Q9 and Q11 to Q13 = LOW), independent of other input conditions. In the HCT version, the MR input is TTL compatible, but the RS input has CMOS input switching levels and can be driven by a TTL output by using a pull-up resistor to V_{CC}.

2. Features

- All active components on chip
- RC or crystal oscillator configuration
- Complies with JEDEC standard no. 7 A
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Applications

- Control counters
- Timers
- Frequency dividers
- Time-delay circuits

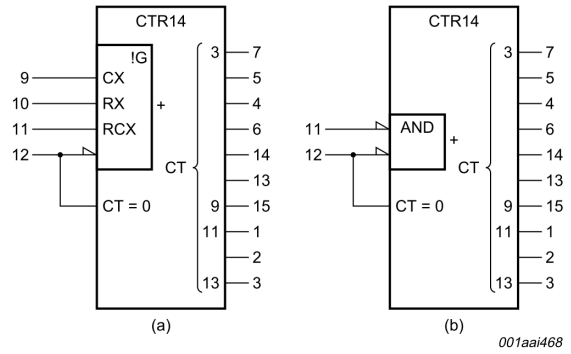


Fig 2. IEC logic symbol

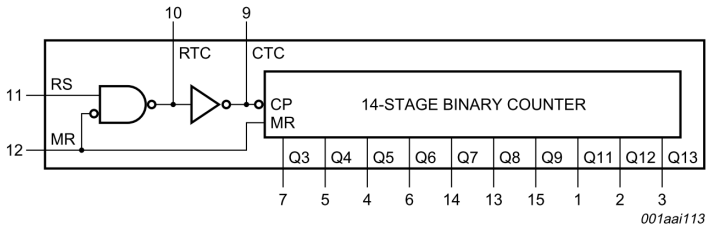


Fig 3. Functional diagram

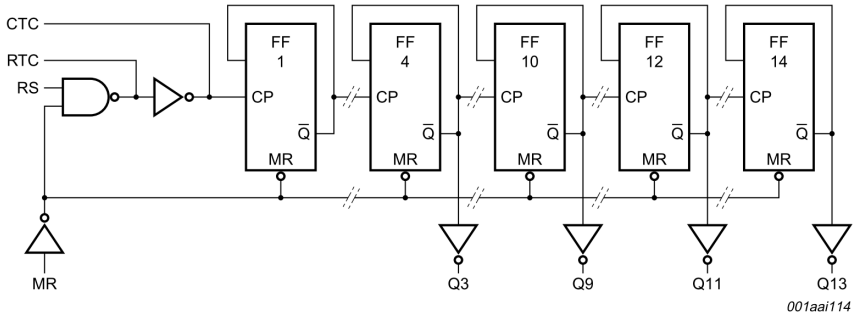


Fig 4. Logic diagram

6. Pinning information

6.1 Pinning

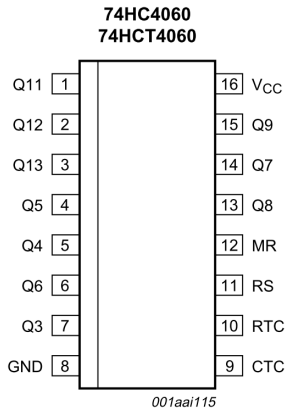
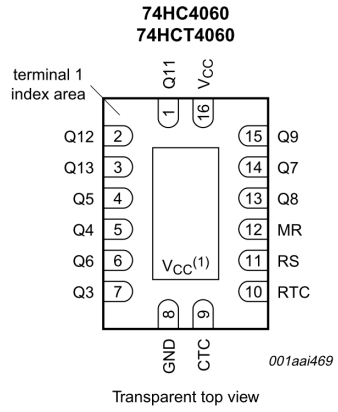


Fig 5. Pin configuration DIP16, SO16 and (T)SSOP16



(1) The die substrate is attached to this pad using conductive die attach material. It cannot be used as supply pin or input.

Fig 6. Pin configuration DHVQFN16

6.2 Pin description

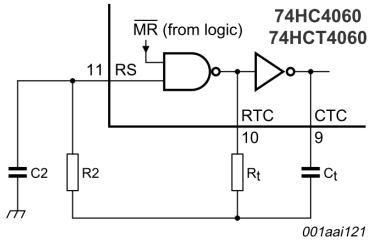
Table 2. Pin description

Symbol	Pin	Description
Q11 to Q13	1, 2, 3	counter output
Q3 to Q9	7, 5, 4, 6, 14, 13, 15	counter output
GND	8	ground (0 V)
CTC	9	external capacitor connection
RTC	10	external resistor connection
RS	11	clock input /oscillator pin
MR	12	master reset input (active HIGH)
V_{CC}	16	supply voltage

13. RC oscillator

13.1 Timing component limitations

The oscillator frequency is mainly determined by R_tC_t, provided R2 ≈ $2R_t$ and R2C2 << R_tC_t. The function of R2 is to minimize the influence of the forward voltage across the input protection diodes on the frequency. The stray capacitance C2 should be kept as small as possible. In consideration of accuracy, C_t must be larger than the inherent stray capacitance. R_t must be larger than the ON resistance in series with it, which typically is 280 Ω at V_{CC} = 2.0 V, 130 Ω at V_{CC} = 4.5 V and 100 Ω at V_{CC} = 6.0 V.



Typical formula for oscillator frequency: $f_{osc} = \frac{1}{2.5 \times R_t \times C_t}$

Fig 12. Example of a RC oscillator

The recommended values for these components to maintain agreement with the typical oscillation formula are:

C_t > 50 pF, up to any practical value and 10 kΩ < R_t < 1 MΩ.

In order to avoid start-up problems, R_t ≥ 1 kΩ.

13.2 Typical crystal oscillator circuit

In Figure 13, R2 is the power limiting resistor. For starting and maintaining oscillation a minimum transconductance is necessary, so R2 should not be too large. A practical value for R2 is 2.2 kΩ.